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(54) Mobile communications apparatus with digital clock recovery

(57) Mobile communications apparatus with digital clock recovery comprises a circuit receiving an input signal (14) and using a digital clock (16) to provide a signal containing a measure of input phase, and further comprises an integrator (26) providing a phase measurement signal, followed by a differentiator (30) which provides a frequency measurement signal for enhancing the phase measurement signal used to lock the system to enable accurate data sampling. The frequency measurement signal enhances the phase measurement signal by i) modifying that signal by adding the frequency measurement signal (divided by a selected factor) to the phase measurement signal and/or ii) providing an alternative integrator input. In the absence of a stable input phase measurement signal for longer than a given period, the frequency measurement signal is fed to the integrator in place of the input phase measurement signal.

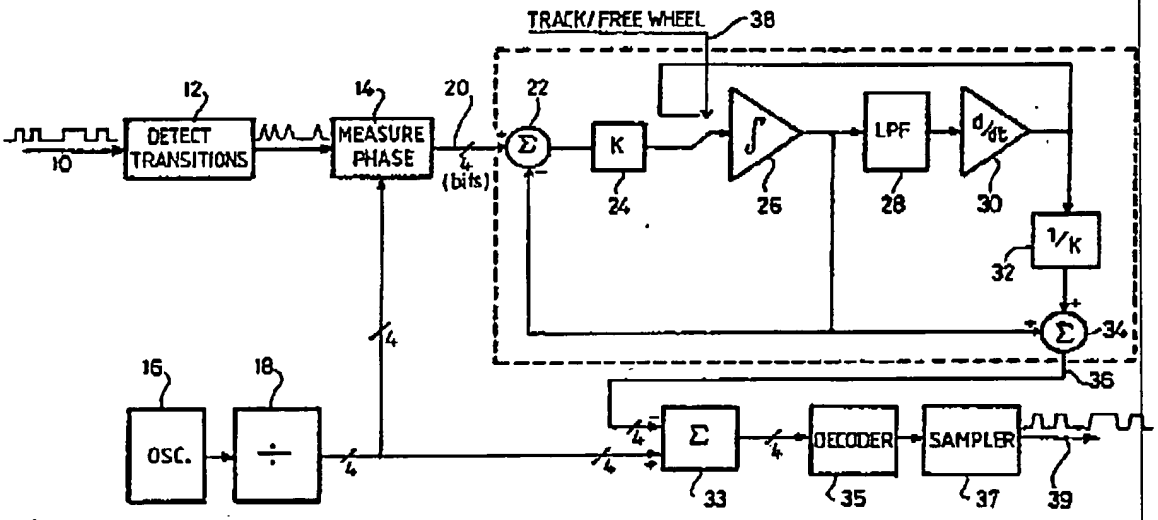

Fig. 3

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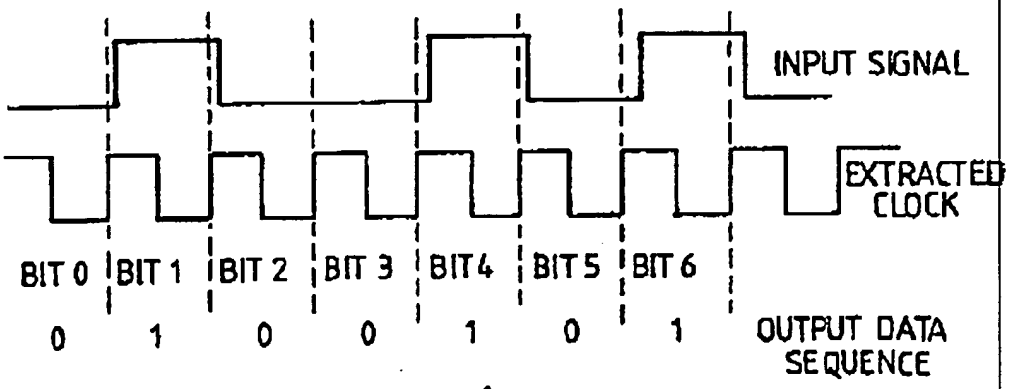
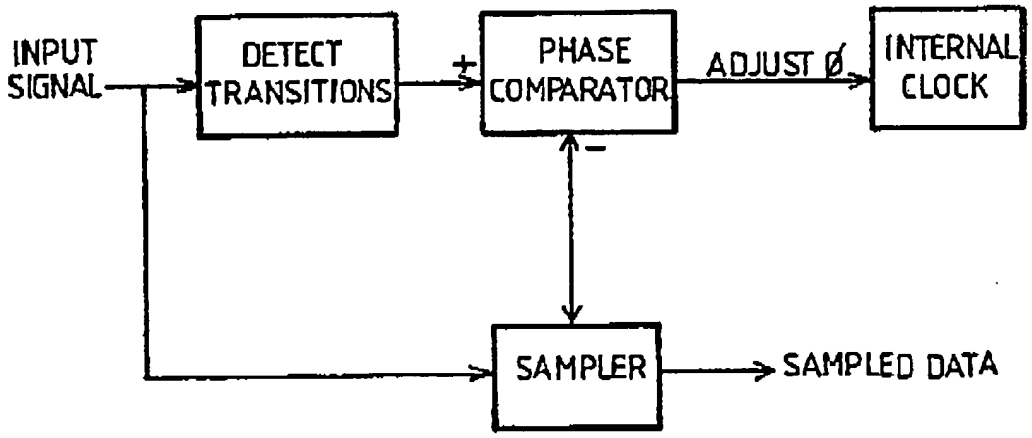


Fig. 1



PRIOR ART

Fig. 2

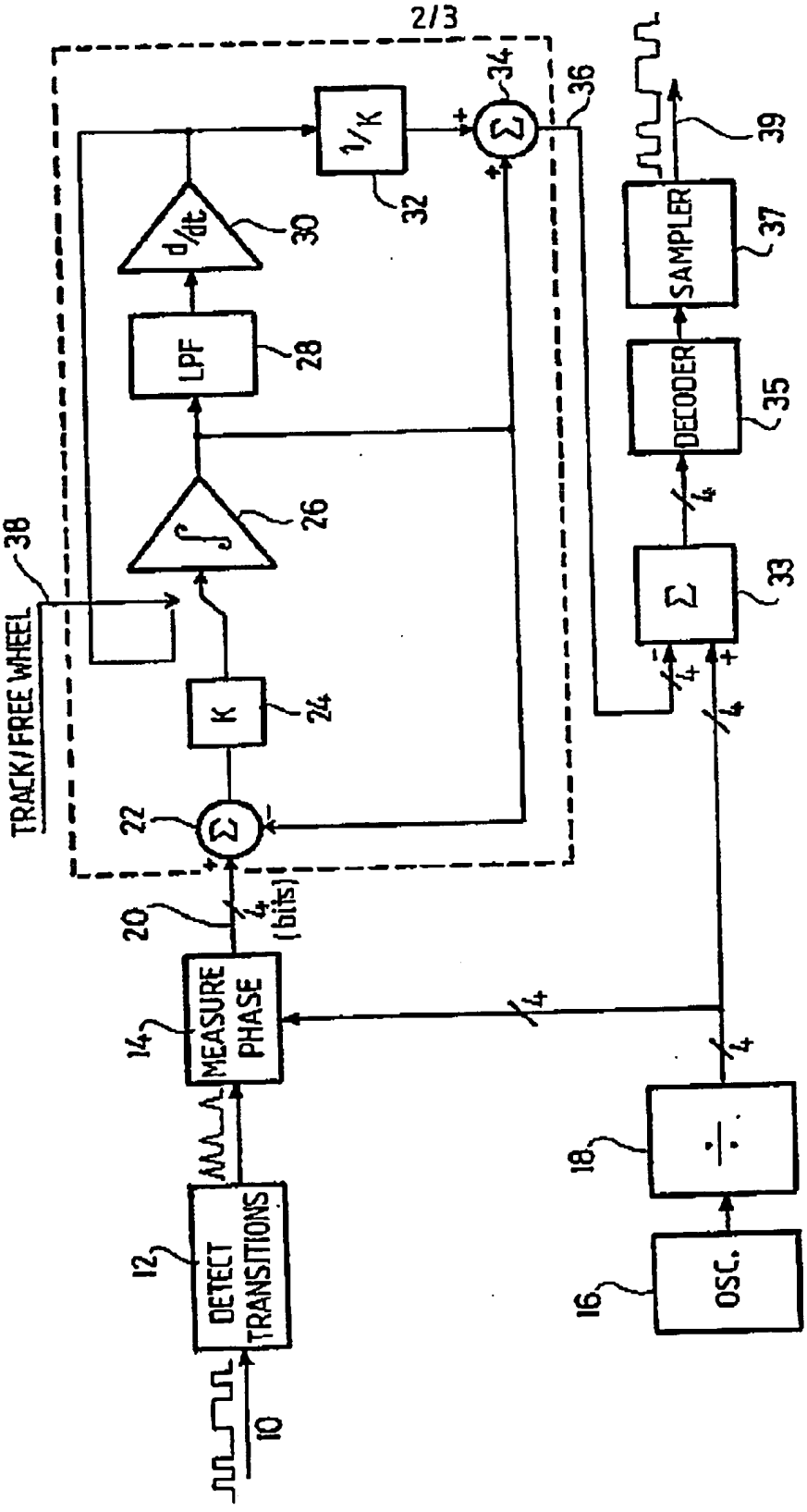

2/3
10
DETECT TRANSITIONS
12
MEASURE PHASE
14
OSC.
16
÷
18
4 (bits)
20
Σ
22
K
24
∫
26
LPF
28
d/dt
30
1/K
32
Σ
33
DECODER
35
SAMPLER
37
39
34
36
38
TRACK/FREE WHEEL

Fig. 3

3/3

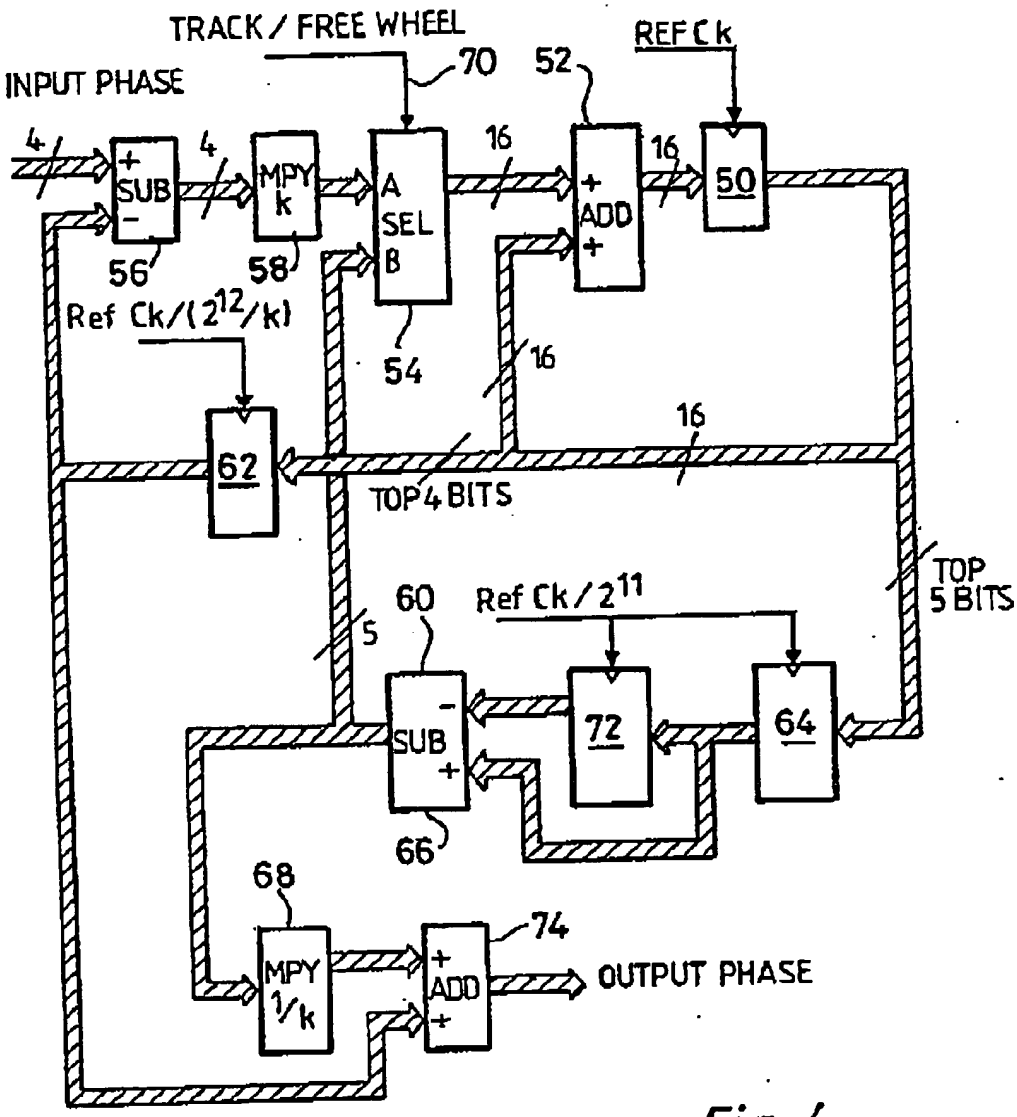

TRACK / FREE WHEEL
INPUT PHASE
70
52
REF Ck
4
4
16
16
SUB
MPY k
A SEL B
ADD
50
56
58
54
Ref Ck/(2^12/k)
16
16
62
TOP 4 BITS
TOP 5 BITS
60
Ref Ck/2^11
5
SUB
72
64
66
68
74
MPY 1/k
ADD
OUTPUT PHASE

Fig. 4

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Mobile Communications Apparatus with Digital Clock Recovery

This invention relates to mobile communications apparatus, e.g. a cordless telephone, having digital clock recovery.

In a cordless telephone, for example, the received digital signal comprises a series of loosely shaped pulses of a length approximately corresponding to a fundamental time period or integral multiple thereof occurring at intervals equal to or an integral multiple of the fundamental time period, which is itself dependent on the fundamental frequency of the signal. The signal pulses are squared, and the sequence of digital 0s and 1s represented by the squared pulses is extracted.

A conventional method of extraction is digital clock recovery. An internal clock is employed to generate a clock signal of frequency and phase matching the positions of the transitions in the input signal, i.e. matching the pulse edges. The input signal is then sampled mid-way in the clock cycles.

Figure 1 of the accompanying drawings illustrates the digital clock recovery process, and Figure 2 is a block diagram of a conventional digital clock extraction circuit. The phase comparator with feedback from the internal clock is provided to continually adjust the phase of the clock signal, i.e. phase lock the clock signal to the input signal, in an endeavour to overcome three main problems:-

a) jitter at the bit boundaries;

b) maintenance of locking of the clock signal to the

input signal even when a long period occurs without a bit transition; and

c) the occurrence of bursts of noise.

Known implementations of the basic circuit of Figure 2 are not wholly successful in overcoming the problems mentioned above, and it is an object of this invention to provide an improved apparatus with digital clock recovery.

According to the invention, mobile communications apparatus with digital clock recovery comprises circuit means receiving the input signal and utilising a digital clock to provide a signal which contains a measure of the input phase, a feedback loop including an integrator which generates a signal containing a phase estimate and which is fed back to a subtractor which also receives the signal containing the input phase measure, the output of the subtractor being fed after amplification to the input of the integrator, a differentiator which receives the output of the integrator through a low-pass filter, the output of the differentiator providing a signal containing a frequency estimate of the input signal relative to the clock signal, and circuit means whereby the frequency estimate signal is utilised to modify the phase estimate signal and/or to provide an alternative input to the integrator.

It is known from the prior art to combine phase locking with frequency locking of the clock signal to the input signal, but the present invention aims to provide an improved and more versatile means for practising phase and frequency locking.

Further features and advantages of the mobile communications

apparatus of the invention will be apparent from the following description of an embodiment, making reference to the accompanying drawings, in which:-

Figures 1 and 2 show prior art;

Figure 3 is a block circuit diagram of the complete apparatus, including within the dashed-line box improved circuitry in accordance with the invention: and

Figure 4 shows a preferred embodiment of the circuitry contained in the dashed-line box of Figure 3.

Referring to Figure 3, the input signal 10 containing the pulses to be sampled is fed to a transition detector 12 generating a signal containing spikes corresponding to the signal pulse transitions. The spike-containing signal then passes to a phase measurement circuit 14 which also receives a four bit input from a digital clock comprising a crystal oscillator 16 and divider 18. The output of circuit 14, which latches the continuously changing spike count, is a four bit signal 20 containing a measure of the input phase, all in accordance with conventional practice. The invention is particularly concerned with the handling of the input phase measurement signal 20. This signal is fed into a first order tracking loop which comprises a subtractor 22 receiving the input phase measurement signal and a phase estimate signal. The subtractor generates a phase error signal fed through a constant gain amplifier 24 to an integrator 26, which provides at its output the phase estimate signal fed back to the subtractor 22.

The output of the integrator 26 is also fed via a low-pass

filter 28 to a differentiator 30, which produces a signal containing an estimate of the difference between the frequency of the input signal and the reference clock rate. This frequency estimate signal lags behind the input phase measurement signal by an amount proportional to the frequency error and is therefore divided at a divider 32 by a factor k, to provide offset compensation, before being fed to an adder 34 which also receives the phase estimate signal from the integrator. The adder 34 thus provides as an output a signal 36 containing an improved phase estimate.

The output signal 36 is handled substantially conventionally by means of a subtractor 33, decoder 35 and sampler 37, to provide the output 39 of sampled data.

When there is no input phase information available, a "Track/Free Wheel" input 38, in itself forming no part of the present invention, may be used to assist in maintaining locking. The input to the integrator 26 is taken, not from the input phase error signal, but from the frequency estimate signal output from the differentiator 30. The output from the integrator 26 then ramps up or down at a constant rate corresponding to the frequency estimate. The improved phase estimate signal 36 will thus also ramp at a constant rate. Thus, in the absence of input phase information, the extracted clock phase is made to ramp up or down at a rate corresponding to the frequency error that was previously present, between the input bit rate and the reference clock rate.

It is desirable to make the gain factor k variable. During clock acquisition, a large value of k causes the system to gain lock more rapidly because the loop bandwidth is increased. At the same time, this reduces the influence

of the frequency estimate signal, which may not yet have stabilised. When the system has gained lock, the value of k can be progressively reduced so that loop bandwidth is reduced and a greater averaging is done on the input clock phase, making the system less prone to transient disturbances. The effects of lag in the system are then counteracted by the greater offset compensation achieved by the divider 32.

Offset compensation may be conditional. The multiplication of the output of the differentiator 30 by 1/k and its addition to the phase estimate is only essential if the phase offset resulting from a frequency error is excessive. If the frequency error is small relative to the tracking bandwidth of the integrator loop, phase offset compensation need not be effected.

In general, the circuit elements within the dashed-line box of Figure 1 can be designed using modulo arithmetic, i.e. arithmetic in which overflows and underflows are ignored. By appropriate selection of digital word widths and values the circuit elements can be made relatively simple. For instance, the integrator may be designed so that its wrap-around corresponds to the wrap-around of the phase estimate at 360°. The use of modulo arithmetic is illustrated by the preferred embodiment shown in Figure 4, which replaces the circuitry within the dashed-line box of Figure 3.

In Figure 4, the functional blocks represent standard logic circuits such as adders and latches. The circuit as a whole is intended to be implemented using a gate array or standard cell design.

The integrator consists of latch 50 and adder 52. Thus,

upon each positive edge of the reference clock (Ref Ck), the output of the adder 52 equals the old output plus the output from data selector 54 which has an input from subtractor 56 via multiplier 58 and an input from subtractor 60. Over a number of clock cycles, the output of the data selector 54 is integrated. The output of the integrator 50, 52 is latched every so many cycles ($2^{12}/k$ cycles) to give an updated phase estimate. Because it is the top bits of the integrator output that are used as the phase estimate, overflow of the integrator corresponds to the phase transition 358°, 359°, 0°, 1° ... and overflow and underflow of the arithmetic can be ignored.

The phase error is integrated between one clocking of latch 62 and the next. If the integrator 50, 52 is cleared every time latch 62 is clocked, the output of latch 62 will measure the average phase error over the period. This is a fast manner in which to bring the system into locked condition, because the phase error is reduced to zero at the instant that latch 62 is clocked.

The latch 62 has the further advantage that the arithmetic of circuit elements 56, 58, 54 and 52 is simplified. For example, if k = 1 and the phase error is constant at -1 represented by 1111 in binary, then with the integrator 50, 52 cleared initially, the next time latch 62 is clocked, the integrator 50, 52 contains F000 (hexadecimal) so the fed back phase estimate is 1111, which is correct. It is to be noted that the integrator can perform this function without having to represent the 16 bit binary number between selector 54 and adder 52 as a negative number; only the four significant bits need be used.

A minor disadvantage of the latch 62 is that it restricts

the update rate of the phase estimate. For small values of k (multiplication factor), a moderate frequency error of, say, 100 ppm, will cause the phase to alter by two or three units between updates. Such an error would not be acceptable; a satisfactory compromise is to employ latch 62 to promote fast locking and then by-pass the latch when a longer time constant is required.

The factor k controls the loop bandwidth. In this system k starts at a value of 9, enabling the system to gain lock after about 8 bit transitions. k is progressively reduced to slow the response of the system so that it averages the input phase over thousands of cycles in the process of updating its phase estimate.

Latches 62 and 64, together with subtractor 66, estimate the frequency error. The frequency is estimated as the change in phase over 2^{11} clock cycles (see divider 72). The frequency estimate is of poor accuracy when the loop bandwidth is high. However, the multiplier 68 (factor 1/k) suppresses the effect of frequency compensation under such circumstances. When the system has locked and the bandwidth has been reduced, frequency compensation is required. By now, however, the frequency estimate is very good and the frequency compensation achieved will be reliable. It is to be noted that underflow caused by wrap around in the integrator does not affect the output of the frequency estimator as long as the frequency error is small enough not to go beyond the word width assigned to it.

When free-wheel 70 is selected, the integrator 50, 52 is up-dated with the estimated frequency instead of the input phase error. This causes the integrator to ramp at a continuous rate, so tracking the phase when there is a

frequency error but input phase information is temporarily unavailable.

The free-wheel input is typically used during periods when it is known that there is no valid data, when a bit transition has occurred outside an acceptance window, or if a period of erratic input phase has been identified.

The multiplication factor k is chosen to be an integral power of 2, so that the multiplications are implemented as shifts. By varying k, the bandwidth of the system is altered. The internally stored value of the phase remains valid even when the bandwidth is switched, so that the system does not lose phase locking.

The output-phase signal is provided by adder 74.

Various modifications of the above-described and illustrated arrangement are possible within the scope of the invention defined by the appended claims.

Claims

1. Mobile communications apparatus with digital clock recovery, comprising circuit means receiving the input signal and utilising a digital clock to provide a signal which contains a measure of the input phase, a feedback loop including an integrator which generates a signal containing a phase estimate and which is fed back to a subtractor which also receives the signal containing the input phase measure, the output of the subtractor being fed after amplification to the input of the integrator, a differentiator which receives the output of the integrator through a low-pass filter, the output of the differentiator providing a signal containing a frequency estimate of the input signal relative to the clock signal, and circuit means whereby the frequency estimate signal is utilised to modify the phase estimate signal and/or to provide an alternative input to the integrator.

2. Mobile communications apparatus as claimed in claim 1, wherein the last recited circuit means comprises means for adding the frequency estimate signal to the phase estimate signal.

3. Mobile communications apparatus as claimed in claim 2, in which, before adding to the phase estimate signal, the frequency estimate signal is divided by a selected factor.

4. Mobile communications apparatus as claimed in claim 3, wherein said division factor is variable.

5. Mobile communications apparatus according to claim 4, wherein the division factor is progressively reduced after achievement of phase locking.

6. Mobile communications apparatus according to any of claims 1 to 5, wherein, in the absence of a stable input phase measurement signal for longer than a given period, the frequency estimate signal is fed back to the integrator in place of said input phase measurement signal.

7. Mobile communications apparatus according to claim 6, wherein the integrator simultaneously receives a track/free wheel input signal.

8. Mobile communications apparatus according to any of claims 1 to 7, wherein the phase feedback loop circuitry and the frequency estimating circuitry are constituted by circuit elements functioning in accordance with modulo arithmetic.

9. Mobile communications apparatus according to claim 8, wherein the integrator comprises an adder and a latch receiving the clock signal, the adder receiving inputs from a data selector and the latch, and the data selector receiving the phase measurement signal after multiplication thereof and an input from a subtractor providing the frequency measurement signal.

10. Mobile communications apparatus according to claim 9, wherein the subtractor receives inputs from a clock signal divider and a second latch which receives an input derived from the clock signal.

11. Mobile communications apparatus according to claim 10, wherein the phase measurement signal is output through a latch receiving a signal derived from the clock signal and providing an output to an adder which also receives the frequency measurement signal through a divider.

12. Mobile communications apparatus substantially as hereinbefore described with reference to Figure 3 or Figure 4 of the accompanying drawings.

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